In the Claims

23. (Amended) The field effect transistor of claim 22 wherein said heavily doped semiconductor regions include [SiGe alloy] a material selected from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$ and SiGe.

Add new Claims:

37. The field effect transistor of claim 30 wherein said spaced apart metal-semiconductor compound regions further include an additional layer of conductive material between said metal and said first dielectric layer, said additional layer of conductive material having sidewalls, said sidewalls having an insulating material disposed thereon.

38. The field effect transistor of claim 37 wherein said additional layer of conductive material includes an oxidizable material.

39. The field effect transistor of claim 37 wherein said additional layer of conductive material is selected from the group consisting of Al, Co, Er, Ni, Pd, Pt, Rh, Ta, Ti and W.

40. The field effect transistor of claim 37 wherein said metal of said metal-semiconductor compound regions is selected from the group consisting of Al, Co, Er, Ni, Pd, Pt, Rh, Ta, Ti and W.

41. The field effect transistor of claim 37 wherein said two spaced apart metal-semiconductor compound regions include Ta and said additional layer of conductive material includes Al.

42. The field effect transistor of claim 37 wherein said insulating material disposed on said sidewalls of said additional layer of conductive material also covers sidewalls of said first dielectric layer.

43. The field effect transistor of claim 37 wherein said insulating material disposed on said sidewalls of said additional layer of conductive material includes an oxide of said additional conductive material.

44. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a metal layer on said substrate, said metal layer including material suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said metal layer,

forming a gate opening in said insulating layer to expose said metal layer,

forming a gate dielectric in said gate opening by oxidation of said metal layer,

forming a conductive layer on said gate dielectric in said gate opening, and

patterning said conductive layer to define a gate electrode,

said Schottky metal-to-semiconductor barrier on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

45. The method of claim 44 wherein said step of forming a gate dielectric by oxidation includes the step of electrochemical anodic oxidation of said metal layer.

46. The method of claim 44 wherein said step of forming a gate dielectric by oxidation includes the step of gaseous plasma anodization.

47. The method of claim 44 wherein said step of forming a gate dielectric by oxidation includes the step of heating said metal layer in a reactive ambient to a temperature above a selected temperature.

48. The method of claim 45 further including the step of heating said metal layer in an ambient to a temperature above a selected temperature.

49. The method of claim 46 further including the step of heating said metal layer in an ambient to a temperature above a selected temperature.

50. The method of claim 44 further including the step of forming an additional layer of conductive material over said metal layer after said step of forming a metal layer.

51. The method of claim 50 further including the step of forming an insulating material on exposed sidewalls of said additional layer of conductive material.

52. The method of claim 51 wherein said step of forming an insulating material includes the step of electrochemical anodic oxidation of exposed sidewall regions of said additional conductive material.

53. The method of claim 51 wherein said step of forming an insulating material includes the step of gaseous plasma anodization of exposed sidewall regions of said additional conductive material.

54. The method of claim 51 wherein said step of forming an insulating material includes the step of heating said conductive material in a reactive ambient to a temperature above a selected temperature.

55. The method of claim 52 further including the step of heating said conductive material in an ambient to a temperature above a selected temperature.

56. The method of claim 53 further including the step of heating said conductive material in an ambient to a temperature above a selected temperature.

57. The method of claim 51 wherein said step of disposing an insulating material includes the step of depositing a thin conformal layer of said insulating material in said gate opening and anisotropically etching said insulating material to form 37.

58 The field effect transistor of claim 9 wherein said spaced apart Schottky metal-semiconductor compound regions further include an additional layer of conductive material between said metal and said first dielectric layer, said additional layer of conductive

material having sidewalls, said sidewalls having an insulating material disposed thereon.

59. The field effect transistor of claim 58 wherein said insulating material includes an extension of said gate dielectric layer.

60. The field effect transistor of claim 58 wherein material of said gate dielectric layer is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon oxide/silicon nitride composites, and an oxide, nitride, or oxynitride of Al, Er, Hf, Nb, Ta, Ti, W, Y and Zr and mixtures thereof.

61. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming at least one conductive layer on said substrate, said at least on conductive layer including a metal suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said at least one conductive layer,

forming a gate opening in said at least one conductive layer and said insulating layer,

forming a gate dielectric in said gate opening,

forming a second conductive layer on said gate dielectric in said gate opening, and

patterning said second conductive layer to define a gate electrode,

said Schottky metal-to-semiconductor barrier on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

62. The method of claim 61 further including the step of forming an insulating material on exposed sidewalls of said at least one layer of conductive material.

63. The field effect transistor of claim 9 further including a raised epitaxial channel on said substrate, said raised epitaxial channel formed between said Schottky metal semiconductor compound regions forming said source and drain.